

Serial No. 09/222,524
Docket No. NEC N98039 CON
Amendment G under Rule 116

AMENDMENTS TO THE CLAIMS:

Please amend claims 21-23, 27-29, 33-35 and 39-41..

This listing of claims will replace all prior versions and listings of claims in the
Application:

Claims 1-20 (previously cancelled)

Claim 21 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said wiring substrate having a number of through-holes; and

a number of bumps formed respectively in said through-holes of said wiring substrate in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

~~an external bump pad for said bump electrically connected to said at least two chip electrodes.~~

Claim 22 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of

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Serial No. 09/222,524
Docket No. NEC N98039 CON
Amendment G under Rule 116

said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said wiring substrate having a number of through-holes; and

a number of bumps formed respectively in said through-holes of said wiring substrate in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 23 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having a number of through-holes; and

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; and

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 24 (previously added): A semiconductor device according to claim 21, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Cont
G1

Serial No. 09/222,524
Docket No. NEC N98039 CON
Amendment G under Rule 116

Claim 25 (previously added): A semiconductor device according to claim 22, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 26 (previously added): A semiconductor device according to claim 23, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 27 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side; and

a number of bumps disposed on said wiring of said wiring substrate respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 28 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said wiring substrate, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position; and

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Serial No. 09/222,524
Docket No. NEC N98039 CON
Amendment G under Rule 116

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; ~~and~~

~~an external bump pad electrically to said at least two chip electrodes.~~

Claim 29 (currently amended): A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes; and

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said wiring substrate with said at least two chip electrodes; ~~and~~

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 30 (previously added): A semiconductor device according to claim 27, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 31 (previously added): A semiconductor device according to claim 28, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

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Serial No. 09/222,524
Docket No. NEC N98039 CON
Amendment G under Rule 116

Claim 32 (previously added): A semiconductor device according to claim 29, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 33 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

said TAB tape having a number of through-holes; and

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 34 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring of said TAB tape is bent at at least one position;

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Amendment G under Rule 116

said TAB tape having a number of through-holes; and

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; ~~and~~

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 35 (currently amended): A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring of said TAB tape has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having a number of through-holes; and

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; ~~and~~

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 36 (previously added): A semiconductor device according to claim 33, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

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Serial No. 09/222,524
Docket No. NEC N98039 CON
Amendment G under Rule 116

Claim 37 (previously added): A semiconductor device according to claim 34, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 38 (previously added): A semiconductor device according to claim 35, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 39 (currently amended): A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side; and

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; and

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 40 (currently amended): A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position; and

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Docket No. NEC N98039 CON
Amendment G under Rule 116

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; ~~and~~

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 41 (currently amended): A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer of said semiconductor chip, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes; and

a number of bumps disposed on said wiring of said TAB tape respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring of said TAB tape with said at least two chip electrodes; ~~and~~

~~an external bump pad electrically connected to said at least two chip electrodes.~~

Claim 42 (previously added): A semiconductor device according to claim 39, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 43 (previously added): A semiconductor device according to claim 40, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

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Serial No. 09/222,524
Docket No. NEC N98039 CON
Amendment G under Rule 116

Claim 44 (previously added): A semiconductor device according to claim 41, wherein said chip electrodes comprise at least one kind of terminals selected from ground, power-source and signal terminals of said semiconductor chip.

Claim 45 (previously added): A semiconductor device according to claim 21, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 46 (previously added): A semiconductor device according to claim 22, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 47 (previously added): A semiconductor device according to claim 23, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 48 (previously added): A semiconductor device according to claim 27, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 49 (previously added): A semiconductor device according to claim 28, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 50 (previously added): A semiconductor device according to claim 29, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

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Amendment G under Rule 116

Claim 51 (previously added): A semiconductor device according to claim 33, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 52 (previously added): A semiconductor device according to claim 34, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 53 (previously added): A semiconductor device according to claim 35, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 54 (previously added): A semiconductor device according to claim 39, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 55 (previously added): A semiconductor device according to claim 40, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

Claim 56 (previously added): A semiconductor device according to claim 41, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

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